CLAIMS

1. Circuit testing equipment comprising:

a computer having stored thereon a boundary scan description language (BSDL) file, a netlist and a connections list; and

a connector for connecting the computer to a boundary scan bus of a circuit to be tested;

the computer being arranged to parse the BSDL file, the netlist and the connections list and generate a data structure therefrom which, when combined with a test script, permits execution of the test script from the computer through the boundary scan bus.

2. The equipment of claim 1, wherein the computer has all information necessary to identify whether, for a given pin, a BSDL file is present and whether the given pin is connected through the netlist to a pin of a device for which a BSDL file is present, whereby the pin can be controlled using the boundary scan bus.

3. Equipment according to claim 1, wherein the computer comprises a parser for parsing the BSDL file, the netlist and the connections, and a compiler for compiling the same to generate the data structure for execution with the test script.

4. Equipment according to claim 1, wherein the computer further comprises at least one test script for testing an integrated circuit of the circuit to be tested.

5. Equipment according to claim 1, for testing a circuit that has at least one boundary-scan capable IC, the at least one boundary-scan capable IC having at least a first pin and a second pin, wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state,

the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states.

6. Equipment according to claim 1, wherein the computer further comprises a first test script for testing a first integrated circuit of the circuit to be tested and a second test script for testing a second integrated circuit of the circuit to be tested.

7. Circuit testing equipment according to claim 1 for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable and at least one second IC that is not boundary-scan capable, wherein the data structure defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC.

8. Circuit testing equipment for testing a circuit that has at least one first integrated circuit (IC) that is boundary-scan capable, and at least one second IC that is not boundary-scan capable, the equipment comprising:

an input for inputting files comprising a boundary scan description language (BSDL) file, a netlist and a connections list; and

a data structure generated from the BSDL file, the netlist and the connections list that defines all pins of the first IC that are capable of driving pins of the second IC and all pins of the first IC that are capable of reading pins of the second IC, whereby the second IC and its connections to the first IC can be tested by driving pins of the first IC.

9. Equipment according to claim 7 wherein the first IC has pins that are capable of adopting one of three states, being a high state, a low state and an input state.

10. Equipment according to claim 7 wherein the first IC is connected to a boundary scan bus.

11. Equipment according to claim 7, further comprising a parser and a compiler for parsing and compiling the BSDL file, the netlist and the connections list to generate the data structure, wherein the parser and compiler are implemented in computer programs loaded into a computer to be connected to the circuit to be tested.

12. Equipment according to claim 11, wherein the computer further comprises a test script for testing the second IC and its connections to the first IC.

13. Equipment according to claim 8, wherein the at least one first IC has at least a first pin and a second pin, wherein at least the first pin is capable of adopting one of three states, being a high state, a low state and an input state,

the equipment further comprising connection test software arranged to test that the first and second pins are not connected, by setting the first pin to the input state and driving the second pin sequentially into the high and low states.

14. A method of testing an integrated circuit board having a boundary scan test port, the method comprising:

connecting a computer to the boundary scan test port;

loading and parsing a boundary scan description language file, a netlist and a connections list in the computer and compiling these into a data structure for testing a circuit on the board;

loading a test script specific to an integrated circuit (IC) mounted on the board; and

running the test script using the data structure to thereby send to the boundary scan test port selected signals to test selected pins of the integrated circuit.

15. A method according to claim 14, wherein the test script is specific to the IC to be tested but independent of the circuit board on which it is mounted.

16. A method according to claim 14, further comprising the steps of:

performing a loop in the test script;

waiting for a test result; and

executing selected further tests in response to the test result.

17. A method according to claim 16, wherein the further tests are performed when a failure result is returned by the test script and wherein the further tests facilitate identification of the cause of the failure result.

18. A method according to claim 16, wherein the further tests are performed when a success result is returned by the test script, and wherein the further tests omit selected tests that are superfluous only in the event of the success result.

19. A method according to claim 14 further comprising the steps of:

reading first and second data from first and second pins respectively in the circuit board through the boundary scan bus; and

performing a correlation between said first and second data.

20. A method according to claim 14, wherein the IC provides an operation complete output indicating that an operation is complete, and wherein the test script includes a loop to repeatedly check the operation complete output.

21. A method according to claim 20, wherein the test script proceeds from a first test operation to a second test operation when the operation complete output indicates that the first test operation is complete.

22. A method of developing integrated circuit boards, comprising performing the method of claim 14 on a first board, reviewing results of the method, creating a derivative board, and an associated netlist without changing the test script, and performing the method of claim 14 again on the derivative board.